UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,918	11/14/2003	Mitsuyoshi Mori	60188-710	7667

7590 07/24/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,918	MORI ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10,12-31 and 34-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10,12-31 and 34-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 8 May 2006 have been entered and made of record. The objections to claims 6, 18, and 28 have been withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims **37 and 38** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim references a single floating diffusion section and a plurality of pixel amplifiers connected to the FD section The disclosure does not enable a plurality of pixel amplifiers connected to each FD section, nor does it make clear a pair of signal output lines from an amplifier transistor which is adjacent to another amplifier transistor in the row direction. Instead the disclosure shows a single amplifier with a single output line connected to the FD section, shared between transistors in the row direction (item 24 in Fig 1 for example). Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **12-26 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent (previously cited) and Hashimoto (US 6,956,605).

7. Regarding claim **12**, the '869 patent discloses in Figure 3a a solid state imaging apparatus comprising: a plurality of photoelectric elements (PD1a-PD2b) arranged in an array of two rows and two columns; and a plurality of switching elements (TG1a-TG2b) for transferring charges from one of said photoelectric elements.

The '869 patent fails to specify a plurality of a pair of read lines coupled to the switching elements wherein one of the pair of read lines is connected to a switching

element at an odd-numbered column and the other is connected to a switching element at an even-numbered column; and that one of the floating diffusion sections is shared by four photoelectric elements which are adjacent to the floating diffusion section in a row direction and a column direction. Instead the '869 patent shows two floating diffusion areas, shared by two pixels in a column direction but isolated from each other by a reset transistor (37). The '869 patent also shows four separate read lines.

Hashimoto teaches in Fig 2 a floating diffusion section (also Fig 21 item 85) shared by four photoelectric elements (a_{11}-a_{22}), providing a device capable of adding signals from the plurality of photoelectric elements (col 1 ln 46-48). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Hashimoto on the device of the '869 patent in order to create a device capable of adding signals from a plurality of elements, through a common amplifier section. Hashimoto also shows a plurality of a pair of read lines connected to alternating odd (O11) and even (e12) column switching elements.

8. Regarding claim **13**, the '869 patent teaches in Fig 3a the apparatus of device 12, further comprising a reset transistor (37) for resetting charge stored in each said floating diffusion section and a pixel amplifier transistor (32) for detecting and outputting a voltage potential converted from said floating diffusion section; wherein a drain of the reset transistor is connected to a drain of the pixel amplifier transistor so that the drain is shared by the reset transistor and the pixel amplifier transistor (connected to Vdd).

9. Regarding claim **14**, Hashimoto teaches in Fig 21 the apparatus of claim 12 wherein the floating diffusion section (85) is arranged between the two photoelectric elements which are adjacent to each other in the row direction (82a, 82c).

10. With regards to claim **15,** patent '869 discloses in Figure 3b wherein said switching elements are made of an MIS transistor (T_G1b), and a gate of the MIS transistor is arranged in the row direction (Fig 3a).

11. Regarding claim **16**, patent '869 discloses in Figure 3a the apparatus of claim 13 wherein said pixel amplifier transistor (32) is arranged between rows, which include some of the photoelectric elements adjacent to each other.

12. With regards to claim **17**, Hashimoto discloses in Figure 21 the apparatus of claim 13 wherein the pixel amplifier (86) and floating diffusion section (85) are arranged between the first read line (88b) and the second read line (88d).

13. Regarding claim **18**, patent '869 discloses in Figure 3a the apparatus of claim 12, wherein the plurality of photoelectric elements arranged in an array of two columns defines a photoelectric section; and the output transistor (32) is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

14. Regarding claim **19**, patent '869 discloses in Figure 3a the apparatus of claim 15 wherein each pixel amplifier (32) is arranged between the gate of a first MIS transistor (52) and the gate of a second MIS transistor (62).

15. With regards to claim **20**, Hashimoto discloses in Figure 21 the apparatus of claim 13 wherein each said reset transistor (93) is arranged between the first read line (88b and the second read line (88d).

16. Regarding claim **21,** Hashimoto discloses in Figure 21 the apparatus of claim 18, wherein the pixel amplifier (86) and the floating diffusion section (85) are arranged between the two photoelectric sections, which are adjacent to each other.

17. Regarding claim **22**, patent '869 discloses in Figure 3a the apparatus of claim 18, wherein the reset transistor (36) is arranged between the two photoelectric sections, which are adjacent to each other in the row direction.

18. With regards to claim **23**, patent '869 discloses in Figure 3a the apparatus of claim 18 wherein the reset transistor (36) is arranged between the two photoelectric sections, which are adjacent to each other in the column direction.

19. With regards to claim **24**, patent '869 discloses in Figure 3a the apparatus of claim 15 wherein said reset transistor (37) is arranged between the gate of a first MIS transistor (52) and the gate of a second MIS transistor (62).

20. Regarding claim **25**, Hashimoto discloses in Figure 21 the apparatus of claim 18, wherein the floating diffusion section (85) is arranged between the two photoelectric sections that are adjacent to each other in the column direction.

21. With regards to claim **26**, the '869 patent discloses in Figure 21 the apparatus of claim 12, wherein the photoelectric elements are arranged so as to be spaced apart from each other by a certain distance in the row direction.

22. With regards to claim **28**, the '869 patent discloses in Figure 18 the apparatus of claim 13, further comprising a signal processing circuit (73) for processing an output signal from said pixel amplifier transistor.

23. Claims **2-9, 31, and 34-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent and Hashimoto, further in view of Guidash (US 6,552,323), hereinafter the '323 patent.

24. Regarding claim **31**, the '869 patent and Hashimoto disclose each of the elements as recited above with regards to claim 12. The '869 patent and Hashimoto fail to specify a plurality of a pair of read lines coupled to the switching elements wherein one of the pair of read lines is connected to a switching element at an odd-numbered row and an odd-numbered column and a switching elements at an even-numbered row and an even-numbered column, and the other is connected to a switching element at an odd numbered row and an even-numbered column and an even numbered row and an odd numbered column. Instead Hashimoto shows a pair of read lines for each row.

The '323 patent teaches the sharing of pixel output signal lines between adjacent rows of an array, where a pixel output node is shared between row adjacent pixels (col 2 ln 55-57) , in order to realize fill factor improvement (col 2 ln 40-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of the '323 patent of the structure of the '869 patent and Hashimoto, in order to increase the fill factor by sharing output lines between rows of pixels.

25. Regarding claim **35,** patent '869 discloses the apparatus of claim 31, further comprising: an output transistor which is coupled to the first storage node; and the output transistor comprises of a source follower transistor which detects and outputs a voltage potential converted from said first storage node.

26. With regards to claim **36**, the '323 patent discloses in Figure 2c and column 1, lines 40-43 that the apparatus has a plurality of read lines connected to a vertical scanning circuit (x-y addressability).

27. Regarding claim **2**, Hashimoto discloses in Figure 21 the apparatus of claim 31, wherein one element coupled to the first floating diffusion section (85) and one element coupled to the second floating diffusion section are included in the same column (a unit cell is shown, the next row of pixel sections will include an element in column 1 that is connected to a second floating diffusion section).

28. Regarding claim **3**, the '323 patent discloses the apparatus of claim 35 wherein one switching element coupled to the first storage floating diffusion section (first column pair signal line) and one switching element coupled to the second floating diffusion section (second column pair signal line) are included in two adjacent columns (col 2 ln 59-60 and col 4 ln 23-25 recite that each pair of columns shares a signal line, or node). Four columns would include two signal lines, and adjacent columns 2 and 3 would have two different floating diffusion sections.

29. With regards to claim **4**, patent '869 discloses in Figure 3b the apparatus of claim 35, wherein each floating diffusion section (FD) and said pixel amplifier transistor (32) are shared by the two switching elements (T_G1, T_G2) which are coupled to the first and the second read line respectively.

30. Regarding claim **5**, patent '869 discloses in Figure 3b the apparatus of claim 35, further comprising: a signal line (87) for outputting a signal from the pixel amplifier

transistor (32) to the outside; and a select transistor (34) which is provided between the pixel amplifier transistor and the signal line.

31. Regarding claim **6**, patent '869 discloses in Figure 3b the apparatus of claim 34 wherein the first floating diffusion section (FD) and the pixel amplifier transistor (32) are shared by photoelectric elements (PD1a, PD2a), which are adjacent to each other in the row direction (Fig 3a).

32. Regarding claim **7**, Hashimoto discloses in Figure 2 a reset element (MRES) for resetting charge stored in the first floating diffusion section.

33. With regards to claim **8**, the '869 patent discloses in Figure 21 the apparatus of claim 12, wherein the photoelectric elements are arranged so as to be spaced apart from each other by a certain distance in the row direction.

34. Regarding claim **9**, the '323 patent discloses in column 1, lines 40-43, that the apparatus of claim 33 further comprises a signal processing circuit for processing an output signal from said pixel amplifier transistor.

35. With regards to claim **34**, the '323 patent discloses in column 2 lines 25-26 wherein the plurality of photoelectric elements are photo diodes.

36. Claims **29 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent, Hashimoto, and the '323 patent as applied to claim 31 above, and further in view of Patterson (US 6,541,794).

The '869 patent, Hashimoto, and the '323 patent disclose each limitation as claimed in claims 29 and 30 except for disclosing that the solid state imaging apparatus

is part of a camera. Patterson teaches that arrays of photoactive pixel circuits are used in cameras (col 1 ln 11) since they are suitable for capturing images projected onto the arrays (col 1 ln 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Patterson on the array disclosed by the '869 patent, Hashimoto, and the '323 patent in order to capture images.

37. Claims **10 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent, Hashimoto, and the '323 patent as applied to claim 31 above, Patent '869, and further in view of Yamazaki (US 2002/0145582).

The '869 patent, Hashimoto, and the '323 patent discloses each limitation as claimed in claim 31 but do not specify that the sections are separated from one another by a power supply line which also functions as a light-shielding film, or that the shared line (V_{DD}) of the reset transistor and output transistor functions as a light-shielding film.

Yamazaki teaches the use of a power supply line between pixels (or sections), which is also used as a light shield in order to protect the channel formation regions and p type semiconductor regions (¶ 90). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yamazaki on the structure of the '869 patent, Hashimoto, and the '323 patent in order to use the power supply line as a light shield for channel and p type regions between pixels and/or pixel sections. Since V_{DD} is a power supply line, it follows that the shared line of the reset transistor and output transistor would also be used as a light shield.

Response to Arguments

38. Applicant's arguments with respect to the independent claims (12, 29-31) and depending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The relevant patent (6,657,665) discloses an FD section shared between four pixels in a similar arrangement as that claimed in claims 12 and 31.

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John C Ingham
Examiner
Art Unit 2814

jci